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# Sub 20 meV Schottky barriers in metal/MoTe<sub>2</sub> junctions

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## Abstract

The newly emerging class of atomically-thin materials has shown a high potential for the realisation of novel electronic and optoelectronic components. Amongst this family, semiconducting transition metal dichalcogenides (TMDCs) are of particular interest. While their band gaps are compatible with those of conventional solid state devices, they present a wide range of exciting new properties that is bound to become a crucial ingredient in the future of electronics. To utilise these properties for the prospect of electronics in general, and long-wavelength-based photodetectors in particular, the Schottky barriers formed upon contact with a metal and the contact resistance that arises at these interfaces have to be measured and controlled. We present experimental evidence for the formation of Schottky barriers as low as 10 meV between MoTe<sub>2</sub> and metal electrodes. By varying the electrode work functions, we demonstrate that Fermi level pinning due to metal induced gap states at the interfaces occurs at 0.14 eV above the valence band maximum. In this configuration, thermionic emission is observed for the first time at temperatures between 40 K and 75 K. Finally, we discuss the ability to tune the barrier height using a gate electrode.

## 1. Introduction

The emerging class of atomically thin materials has captured the interest of the research community due to the versatile physical phenomena that they exhibit [1, 2]. To name a few, the indirect to direct band gap transition as a function of layer number in atomically thin semiconductors [3], gate-controlled modulation of the band structure in few layer graphene [4] and phase structure transitions [5] hold the key to future innovations in electronic devices. Within this broad spectrum of materials, semiconducting transition metal dichalcogenides (TMDCs) are a major focal point for the wide scientific community working on fundamental and applied aspects of device physics due to their energy gaps of 1–2 eV [6, 7]. These gap values are ideally suited for electronics and optoelectronics, making TMDCs the prime candidates to replace bulk semiconductors in applications where added functionality, such as mechanical flexibility, is required. Atomically thin semiconductors also have the potential to readily form previously hard to access energy barriers, mostly in the few meV regime

[8]. This feature stems from the wide variation in properties (e.g. work function and band gap values [6, 7]) found within the layered materials family. As such, by tailoring the energy barrier formed at the contacts to specific applications, TMDCs can be extremely valuable for light detection in the far infrared regime as internal photoemission diodes [9], replacing other structures that are costly, or difficult to fabricate by any other means.

One approach to realise low energy barriers is by forming a Schottky junction between a TMDC and a metal. Several recent studies on few-layer TMDCs, such as MoS<sub>2</sub>, WSe<sub>2</sub> and MoTe<sub>2</sub> have identified Schottky barriers as the primary contributors to the observed contact resistance [5, 10–15]. Indeed, Guo *et al* showed that metal induced gap states (MIGS) are the primary cause for barrier formation and that the Schottky barrier height (SBH) cannot be significantly altered by changing the work function of the contact metal [10]. In that work the formation of the Schottky barrier has been attributed mainly to the lack of dangling bonds normal to the crystallographic plane of TMDCs. The self terminating plane

means that strong bonds between metal electrodes and the semiconductor cannot be easily formed, a fact that contributes to the increased contact resistance [11]. Experimentally, SBH values of 80 meV were reported with the thermionic emission process being dominant down to 100 K for MoTe<sub>2</sub> [13, 14] and 60 K for MoS<sub>2</sub> [12]. However, lower SBH values have, so far, not been achieved at cryogenic temperatures. At temperatures between 200 and 400 °C, a barrier height of 23 meV has been reported where the MoTe<sub>2</sub> flake is transferred onto pre-defined gold contacts, which may be due to a strain induced structural phase change from semiconducting 2H phase to a metallic 1T' phase at the contacts [16].

Here we report the formation of ultra-low effective SBHs down to 10 meV on MoTe<sub>2</sub>/metal structures, that is aided by Fermi level pinning at the interfaces. MoTe<sub>2</sub> is a TMDC with three different structural phases, the semiconducting 2H, and the semimetallic *T*<sub>d</sub> and 1T' phases. The 2H phase consists of three hexagonal planes in a 'sandwich' formation, with Te at the outer planes and Mo at the centre. These planes are covalently bonded in a trigonal prismatic configuration that constitutes a single layer, and the layers are held together by van der Waals forces [17, 18]. The observed ultra-low effective SBHs in MoTe<sub>2</sub> play a minor role in the conduction at room temperature, but become significant at cryogenic temperatures and manifest in a strongly rectifying behaviour. By analysing the current-voltage characteristics of the conducting channel at different temperatures and various gate biases, we are able to extract its SBH and conductivity values. Within these systems, we find that thermionic emission persists as the dominant mechanism of transport at temperatures that range between 40 K and 75 K, whereas at higher temperatures ( $T \geq 80$  K) other transport mechanisms become more prominent. By varying the electrode material, we show that MIGS pin the Fermi level at the interface at a level of 0.14 eV over the valence band maximum. Finally, we briefly discuss the modulation of the effective SBH with applied gate bias. Our results pave the way for the realisation of far infrared devices in TMDCs and provide insight on the mechanisms of transport in MoTe<sub>2</sub> at cryogenic temperatures.

## 2. Methods

Two terminal field effect devices, schematically shown in figure 1(a) were fabricated by mechanically exfoliating MoTe<sub>2</sub> flakes from a synthetic crystal (*HQ Graphene*) and transferring them onto highly doped silicon substrate with a high quality thermally grown oxide layer. The Si/SiO<sub>2</sub> serves as a global gate electrode and gate dielectric, respectively. Metal contacts were patterned using a regular electron beam lithography procedure immediately prior to metallisation. The devices were then thermally annealed for 2 h in a H<sub>2</sub>/Ar environment at 200 °C.

MoTe<sub>2</sub> flakes were characterised using Raman spectroscopy on a Renishaw Raman microspectrometer using a 532 nm laser. Atomic force microscopy (AFM) micrographs were obtained on an Innova AFM system (*Bruker Inc.*) working in the 'tapping mode', using a Nanosensors high-reflectivity probes operating at a resonance frequency of ~320 kHz, with a nominal radius of curvature of 10 nm or smaller. Once the quality of the flakes were established, the sample was loaded into a helium-3 cryostat, where the source-drain current versus source-drain voltage ( $I_{ds}$ - $V_{ds}$ ) response curves and the source-drain current versus gate-source voltage ( $I_{ds}$ - $V_{gs}$ ) were recorded at decreasing temperatures between 80 K and 40 K using a home-built electrical characterisation setup.

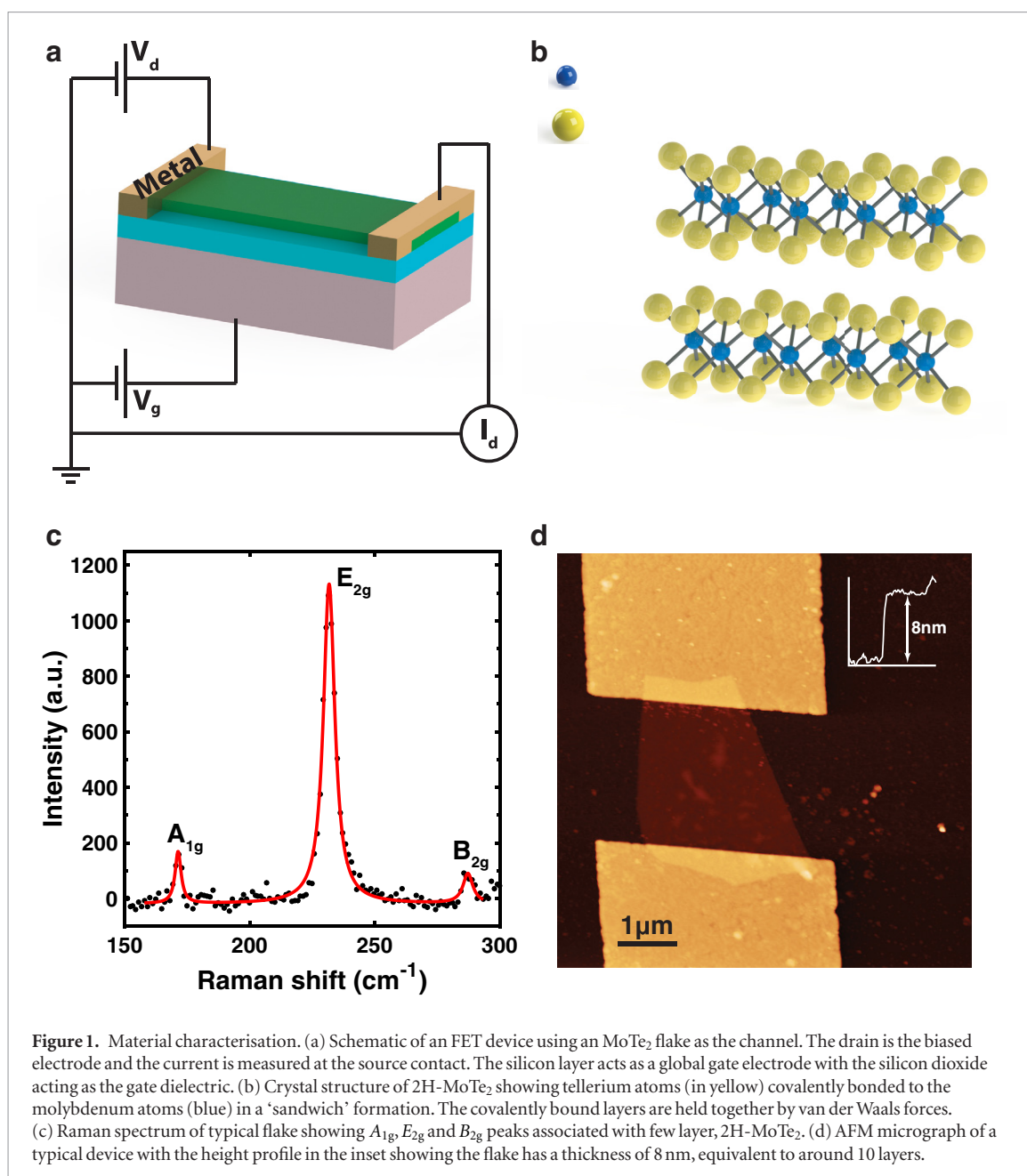
## 3. Results and discussion

The devices, shown schematically in figure 1(a), were characterised using Raman spectroscopy in ambient conditions to ensure that the flakes crystalline structure is the 2H phase (see figure 1(b)). The three peaks in the Raman spectrum (figure 1(c)), at ~170 cm<sup>-1</sup>, ~230 cm<sup>-1</sup> and ~290 cm<sup>-1</sup> are the finger print modes of the 2H phase, namely the *A*<sub>1g</sub>, *E*<sub>2g</sub> and *B*<sub>2g</sub> modes respectively [19–21]. The *B*<sub>g</sub> (~163 cm<sup>-1</sup>) and *A*<sub>g</sub> (~260 cm<sup>-1</sup>) peaks, which are associated with the 1T' phase [19] are absent indicating that the crystalline phase is indeed the semiconducting trigonal structure. As the *T*<sub>d</sub> phase does not exist in room temperature, its Raman peaks are not considered here [22].

The number of layers was determined from the thickness of the flake as measured using atomic force microscopy (AFM). The device topography and structure are shown in the AFM micrograph (figure 1(d)). The cross section profile in the inset of the figure shows that the thickness of the flake is 8 nm, corresponding to 10 layers [21]. All the flakes used in this work were in the range of 5–10 layers.

The few-layer MoTe<sub>2</sub> FET bears two identical metal contacts and should present current response characteristics that are symmetric about the zero source-drain bias ( $V_{ds} = 0$  V). However, the response curve ( $I_{ds}$ - $V_{ds}$ ) shown in figure 2(a) is sub-linear and slightly rectifying, a trend that becomes more pronounced at lower temperatures (figure 2(b)). The increasingly rectifying response to  $V_{ds}$  with decreasing temperature is indicative of the formation of asymmetric Schottky barriers at the interfaces between the metal contacts and the semiconducting channel (see supplementary information section II online ([stacks.iop.org/TDM/5/025023/mmedia](https://stacks.iop.org/TDM/5/025023/mmedia))). While the semiconductor interface potential at the grounded (source) electrode is pinned by the bottom gate, and is effectively a fixed energy barrier, the electrostatic potential of the biased (drain) interface decreases the barrier height with forward bias [23].

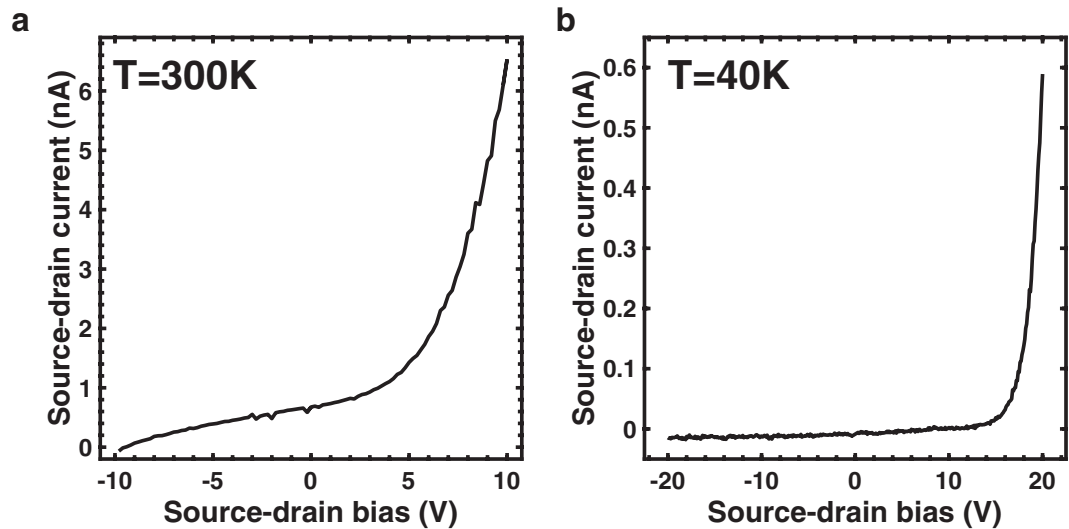
To gain further insights into the response characteristics of the devices, additional electrical



characterisation was carried out in the temperature range from 80 K to 40 K. These measurements were performed at decreasing temperatures to avoid thermal emission of captured charge carriers which would significantly alter the barrier height. The source-drain current versus source-drain bias ( $I_{ds}$ - $V_{ds}$ ) response curves presented in figure 3(a) were measured on a device bearing Au contacts, using an applied gate bias ( $V_{gs}$ ) of  $-40$  V, which is in the devices 'open' state. It is apparent that the device exhibits a highly rectifying diode-like behaviour, which persists at lower temperatures. A graph on a semi-logarithmic scale, plotted in figure 3(b), further emphasises the saturation of the source-drain current when the device is in reverse bias with respect to the source barrier. Other devices displayed similar trends and are shown in supplementary figure S1 online.

Fixing the source-drain bias to a 'forward bias' configuration ( $V_{ds} = +20$  V), the source-drain cur-

rent versus gate bias ( $I_{ds}$ - $V_{gs}$ ) transfer curves were measured, and are plotted in figure 3(c). When the device is forward biased, it exhibits the characteristics of an enhancement type, *p*-channel transistor with its threshold voltage ( $V_{th}$ ) growing increasingly negative with decreasing temperature. The semi-logarithmic scale plot, shown in figure 3(d), shows the subthreshold region where the FET channel switches from its 'closed' state to its 'open' state and enters the linear regime. At 80 K, the two-terminal hole mobility extracted from the linear region of the transfer graph is around  $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , which is in agreement with our previously published devices [24], but lower than the values reported by other groups [25]. We attribute the lower mobility to a high density of interface states, present either at the contacts or across the semiconducting flake. As we will show, this high density of traps contributes to the pinning of the Fermi level at the contacts and is instrumental in the realisation of



**Figure 2.** Response curves at different temperatures. (a) The response ( $I_{ds}$ - $V_{ds}$ ) curve for a device with Au contacts taken at room temperature while the device is in the ‘open’ state at  $V_{gs} = -40$  V. (b) The response curve for the same device taken at 40 K while the rest of the parameters are constant.

ultra-low Schottky barriers. Other devices discussed in this report showed similar trends, see supplementary figure S2 online. Contrary to MoS<sub>2</sub> [26], in MoTe<sub>2</sub> p-type behaviour dominates the transistor characteristics among all the metals used, with the exception of Ti which induces an asymmetric ambipolar behaviour, with p-doping at  $V_{gs} = 0$  V.

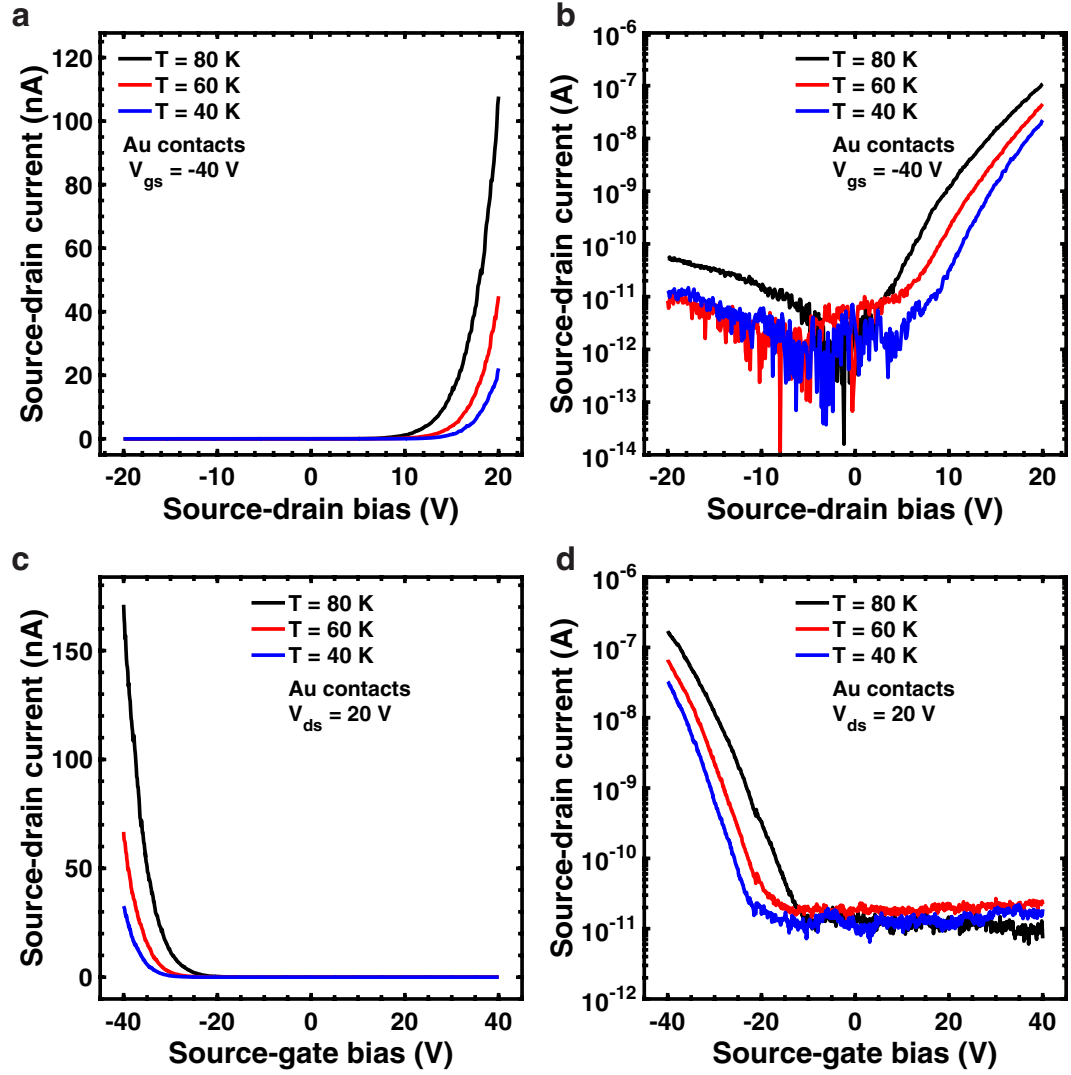
The conductivity dependence on the temperature, determined by the response and transfer curves, which were acquired at different temperatures, reveals that the charge transport is dominated by a thermionic emission over an energy barrier. There are three main mechanisms of transport across an energy barrier: (1) thermionic emission from the high-end tail of Boltzmann distributed particles, (2) diffusion and (3) tunnelling (or field emission) through the barrier [11, 27]. For thermionic emission of charge carriers into a three-dimensional semiconductor, the current dependence with temperature ( $T$ ) is given by the Schottky diode equation  $I = AA^* T^2 \exp(-E_A/kT) [\exp(qV/nk_B T) - 1]$ , where  $A$  is the contact area,  $A^* = 4\pi m^* q k_B^2 / h^3$  is the modified Richardson constant,  $E_A$  is the activation energy required to overcome the barrier,  $n$  is the ideality factor,  $q$  is the basic charge and  $k_B$  is the Boltzmann constant. Other mechanisms of charge transport differ mainly in the exponent of  $T$ , which is 0 for diffusion and 1 for tunnelling. To determine the transport mechanism, the MoTe<sub>2</sub> FET current versus temperature plot shown in figure 4(a) is fitted with  $I_{ds} = B \cdot T^\alpha e^{-C/T}$ , where  $\alpha$  is the exponent of  $T$  used as a fitting parameter and  $B$  and  $C$  are arbitrary constants. The use of the pre-exponential constant is justified by plotting the current at different temperatures with fixed  $V_{ds}$  and fixed  $V_{gs}$ . The extracted  $\alpha = 2.082 \pm 0.211$  is in good agreement with the temperature exponent for thermionic emission, suggesting that this is the dominant

transport mechanism governing the transport in the device, while diffusion and tunnelling of charges play a negligible role in the temperature range between 40 K and 80 K. This is further supported by previous work that has shown the channel is depleted of its majority carriers [24], leading to the formation of barriers as wide as 10  $\mu$ m in MoTe<sub>2</sub> [28], a fact which renders the efficiency of the tunnelling process insignificant. Further discussion on the additional transport mechanisms are included in supplementary information section III online.

For thermionic emission to occur at low temperatures the thermal width of the Fermi–Dirac distribution ( $\Delta E$ ) has to be comparable to or lower than the barrier height.  $\Delta E$  for the majority (80%) of charge carriers can be found using the Fermi–Dirac distribution ( $f(E) = 1/(1 + \exp((E - E_F)/k_B T))$ ) [27] by considering the region between  $f = 0.1$  and  $f = 0.9$ . Within this range, the thermal distribution width is given by  $\Delta E = 4.4 k_B T$ . Supplementary figure S6 online shows the thermal distribution width as a function of temperature. Between the temperatures of 40 K and 80 K, the thermal distribution width ranges from 15 meV to 30 meV. When the thermal energy distribution grows larger than the barrier height, additional mechanisms of charge transfer over an energy barrier, such as tunnelling currents and diffusion, become more prominent, rendering the thermionic emission mechanism irrelevant at higher temperatures.

As previously discussed, the thermionic emission occurs over the source/channel energy barrier that forms when the Fermi energies of the semiconductor and metal reach thermal equilibrium. The surface potential of the metal depletes the adjacent segment of the channel, effectively bending the energy bands of the semiconductor, as shown in figure 4(b), forming the Schottky barrier. In the ideal

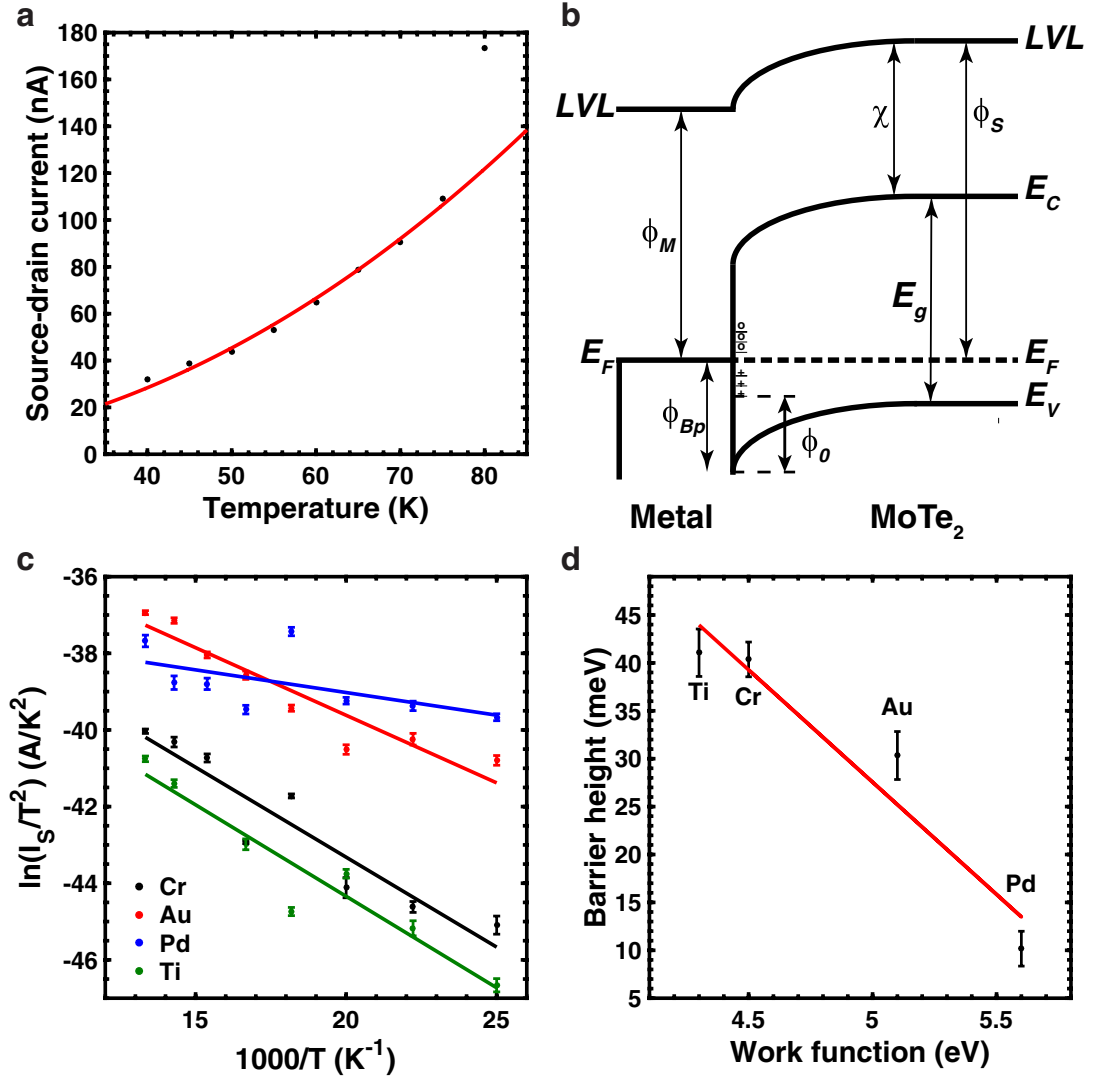




**Figure 3.** Electrical characterisation. (a) Response curves for a device with Au contacts at temperatures between 80 K and 40 K, measured with the devices in the ‘open’ state at  $V_{gs} = -40$  V. The curves exhibit a diode-like rectifying characteristics, as is further emphasised in the semi-logarithmic scale in (b). (c) Transfer curves of the Au contacted device showing the characteristics of an enhancement type, *p*-channel semiconductor with a forward bias of  $V_{ds} = +20$  V. The semi-logarithmic scale in (d) shows a constant current in the subthreshold region.

case the SBH ( $\phi_{BP}$ ) is a function of the metal work function ( $\phi_M$ ), the semiconductor electron affinity ( $\chi$ ) and (for *p*-type materials) the band gap ( $E_g$ ), given by the Schottky–Mott rule,  $\phi_{BP} = E_g + \chi - \phi_M$  [10]. To tune the barrier height, four different metals were used for the contacts, Ti, Cr, Au and Pd with work functions of 4.3 [13], 4.5 [29], 5.1 [29] and 5.6 eV [30] respectively. These work functions should theoretically form barrier heights of 480, 280, −320 and −820 meV respectively, based on an electron affinity of 3.78 eV [31] and a band gap of 1.0 eV [32] for few-layer MoTe<sub>2</sub>. Within this model a negative SBH is indicative of Ohmic contacts. In a realistic interface, mid-gap states, that may be formed by vacancies [10], oxidation [25], and MIGS [33], increase the quantum capacitance of the band gap, an effect known as ‘Fermi level pinning’, effectively altering the barrier height. In the extreme case, known as the Bardeen limit, a large density of mid-gap states can pin the barrier height completely [10].

The MoTe<sub>2</sub> FET exhibits a diode-like behaviour, due to the pinned source/channel potential. As such, we may regard it as a single junction device, while treating the second junction as a fixed resistor. This point is further demonstrated in section 2 of the supplementary information online. In a single diode device, the height of the barrier can be extracted from temperature dependent transport measurements using a Richardson plot [15]. To this end the response curves are fitted with the diode equation  $I_{ds} = I_S \exp(-q(V_{ds} - I_{ds}R_S)/nk_B T) - V_{ds}/R_P$ , where  $R_S$  is a series resistance that includes the channel resistance and the contact resistance and  $R_P$  is a parallel shunt resistance.  $I_S$  is the saturation current which is given by  $I_S = AA^*T^2 \exp(-\phi_{BP}/k_B T)$  for thermionic emission. The extracted  $I_S$  values are then plotted as  $\ln(I_S/T^2)$  versus  $1/T$ , shown in figure 4(c) and supplementary figure S7, which yield effective barrier heights of 41.1, 40.3, 30.3, and 10.2 meV for the Ti, Cr, Au and Pd contacts respectively.



**Figure 4.** Barrier height determination. (a) Current-temperature dependence for an Au contacted device in the ‘open’ state, showing a good agreement with the thermionic emission model for temperatures below 80 K. (b) Schematic energy band diagram of the metal/ *p*-type semiconductor interface showing band bending of the conduction band edge  $E_c$ , the valence band edge  $E_v$  and the local vacuum level  $LVL$  when the Fermi levels  $E_F$  are aligned and the system is in thermal equilibrium. The metal work function  $\phi_M$ , MoTe<sub>2</sub> work function  $\phi_S$ , electron affinity  $\chi$ , band gap  $E_g$  and barrier height  $\phi_{Bp}$  are noted in the diagram. (c) A Richardson plot for the different devices at  $V_{gs}-V_{th} = -11$  V. (d) The relation between barrier height and metal work function from which the extent of  $E_F$  pinning can be determined.

The extraction of Schottky barrier heights as low as a few meVs can cause numerous difficulties due to competing mechanisms of transport. At low temperatures, thermionic field emission can be the dominant mechanism for charge injection into the channel [34]. However, our analysis of the source-drain current versus temperature at fixed source-drain bias and gate bias in figure 4(a) clearly show that thermionic emission is the dominant mechanism. In the determination of the barrier height, we used non-linear implicit function fitting tool to allow the physical parameters  $I_s$ ,  $R_s$ ,  $R_p$  and  $n$  to reach a global minimum of residuals in the parameters space. For this, we have used a step-wise fit [35] to obtain the initial values of the parameters, which were then allowed to reach a higher degree of accuracy. Indeed, the largest source of error in the fittings came from the noise level of the instruments with the small current signal at the lower temperatures.

It is important to note two major consequences of the measured results. First, while the resulting trend is in excellent qualitative agreement with the theoretical case where the barrier height decreases with an increase in metal work function, the extracted effective barrier heights differ profoundly from the calculated values. This indicates significant pinning of the Fermi level by mid-gap states. Second, the measured Schottky barrier heights are comparable with the Fermi Dirac thermal distribution width, thus confirming that thermionic emission over an energy barrier is the dominant current mechanism.

The extent of Fermi level pinning can be quantified by comparing the barrier height with the metal workfunction using  $\phi_{Bp} = \phi_0 + S(\phi_M - \phi_0)$  [10,36], where  $\phi_0$  is the reference energy of the mid-gap states. The pinning factor  $S$  is equivalent to  $-1$  in the ideal case with no pinning (Schottky limit) and



0 if  $E_F$  is completely pinned (Bardeen limit). Figure 4(d) shows that the linear decrease in effective barrier height with increasing metal work function, has a gradient of  $-0.02$  that indicates very strong pinning of the Fermi level. From the intercept of the linear fit, the reference energy of the mid-gap states is found to be  $0.14$  eV above the valence band maximum. The strong pinning also means that gate tunability of the effective Schottky barrier height is considerably suppressed in these devices. Indeed, only the Au and Pd contacted devices show some tunability, exhibiting SBH modulation in the order of up to  $40$  meV for gate bias shifts of  $15$  V. This effect is most likely due to image force barrier lowering, and is discussed in further detail in supplementary figure S8 and the following discussion online in supplementary information section VI, however further work needs to be carried out to fully elucidate this mechanism.

Considering the low charge carrier mobility and the strong Fermi level pinning, we attribute the measured effective barrier heights to the high density of mid gap states present at the metal/semiconductor interface. We have previously shown that slow charge carrier dynamics in  $\text{MoTe}_2$  strongly affects the performance of FETs [24]. However, for photodetectors that are based on internal photoemission of charge carriers between the contact and the channel at that interface, the slow drift of charge carriers does not impede the performance of the detector, and can in fact serve as a short-lived reservoir for excited holes.

## 4. Conclusion

$\text{MoTe}_2$  FETs that exhibit ultra-low effective SBH were presented for the first time. The effective SBH can be controlled by changing the contact metal to some extent, but is dominated mainly by pinning of the Fermi level at the interface. The reference energy of the mid-gap states, which is a measure of the highest energy of occupied mid-gap states, was found to be  $0.14$  eV above the valence band maximum. The tunability of the barrier may assist in the design of internal photoemission based photodetectors, particularly for near-infrared applications.

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